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UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/531,026	03/20/2000	Sudheendra Hangal	16747-01301US	5759

7590 10/06/2003	EXAMINER
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ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 10/06/2003   H

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No. 09/531,026	Applicant(s) HANGAL ET AL.
	Examiner Herng-der Day	Art Unit 2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2000* .

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____ .

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4)☐ Interview Summary (PTO-413) Paper No(s). _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: .

DETAILED ACTION

1.   Claims 1-15 have been examined and claims 1-15 have been rejected.

Priority

2.   Applicants' claim for domestic priority under 35 U.S.C. 119(e) is acknowledged. The provisional application number is 60/127,368, filed April 1, 1999.

Claim Rejections - 35 USC § 112

3.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4.   Claims 1-15 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

For example, as shown in FIG. 3A and FIG. 3B and described in the corresponding specification, each low level simulator run one code fragment which may be of determined length or random length. However, without undue experiment, it is unclear what will happen if the destination of a branch instruction is outside of its current code fragment.

5.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6.   Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing

to particularly point out and distinctly claim the subject matter which applicant regards as the

invention.

6-1.   Claim 4 recites the limitation "set processor" in line 2 of the claim. It is vague and

indefinite about the "set processor" because it does not appear to be supported in the

specification. For the purpose of claim examination, the Examiner will presume that "set

processor" as described in claim 4 refers to "said processor".

Claim Rejections - 35 USC § 103

7.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

8.   Claims 1-2, 4-6, 8-12, and 14-15 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Lauterbach, "Accelerating Architectural Simulation by Parallel Execution of

Trace Samples", Tech. Report SMLI TR-93-22, Sun Microsystems Laboratories, Inc., December

1993, pages 1-14, in view of Applicants' assertions as shown in FIG. 1A.

8-1.   Regarding claims 1 and 8-9, Lauterbach discloses a method for validating performance

and functionality of a processor, comprising the steps of:

(Claim 1) executing a program on a high level simulator of said processor (the entire

execution of the sampled program, page 3, paragraph 3);

establishing a plurality of checkpoints (the start of the sample instruction trace, page 3, paragraph 3; fifty samples, page 3, paragraph 2);

saving state data at each of said checkpoints (initial cache state, page 3, paragraph 3); and

running said program on a plurality of simulators of said processor in parallel, starting each of said simulators at a corresponding checkpoint with corresponding state data associated with said corresponding checkpoint (parallel execution, page 10, section 5.0);

(Claim 8) loading each of said simulators with said program; initializing each of said simulators at said corresponding checkpoint with said corresponding state data associated with said corresponding checkpoint (parallel execution, page 10, section 5.0); and

executing said program on said simulator up to a certain point in said program (250,000 instructions, page 3, paragraph 2).

(Claim 9) said certain point is one of (a) a next checkpoint immediately following said corresponding checkpoint, (b) a point in said program a random length after said corresponding checkpoint, and (c) a point after said corresponding checkpoint (250,000 instructions, page 3, paragraph 2).

However, Lauterbach fails to expressly disclose each of the plurality of simulators is a low level simulator. Nevertheless, Lauterbach suggest existing simulation tools can be leveraged to implement the trace sampling technique (Abstract, page 1, paragraph 2).

Applicants assert, as shown in FIG. 1A and described in pages 1-2 of the specification, "Figure 1A is a block diagram of a prior art processor validation system 100 using only a low level simulator 110" and "One type of low level simulator is the register transfer level (RTL) model of the processor" because "The RTL model is a one hundred percent accurate

representation of a processor and is the same model used to design the processor". However, the low level simulator is very slow such that it is usually infeasible in practice to run long programs on low level simulators.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Lauterbach to incorporate the well known teachings of low level simulator in prior art to obtain the invention as specified in claims 1 and 8-9 because by implementing the trace sampling technique, as suggested by Lauterbach, on the existing RTL simulation tools, it will produce significant reductions in simulation time and still keep one hundred percent accuracy as well.

8-2. Regarding claim 2, Lauterbach further discloses said checkpoints divide said program into code fragments of determined lengths (250,000 instructions, page 3, paragraph 2).

8-3. Regarding claim 4, Lauterbach further discloses said state data comprises:

program counter contents of said processor (Starting PC, page 4, last paragraph);

register contents of said processor (Instruction count, page 4, last paragraph);

cache memory contents of said processor (cache tag state, page 5, paragraph 2);

main memory contents of said processor (TLB tag state, page 5, paragraph 2); and

branch prediction contents of said processor (branch directions, page 5, last paragraph).

8-4. Regarding claim 5, Lauterbach further discloses said processor is one of (a) a microprocessor, (b) a digital signal processor, (c) an input/output (1/O) controller, and (d) a network processor (based on the SPARC™ instruction set, page 3, paragraph 4).

8-5.   Regarding claim 6, Lauterbach further discloses said high level simulator is one of (a) an

instruction accurate simulator (IAS) of said processor and (b) a cycle accurate simulator (CAS)

of said processor (architectural simulation, page 2, paragraph 2).

8-6.   Regarding claim 10, Lauterbach further discloses said running step further comprises

generating one of (a) functional data of said processor and (b) performance data of said processor

(accurate performance estimates, page 2, paragraph 2).

8-7.   Regarding claims 11-12 and 14, these computer readable media claims include same

method limitations as in claims 1-2 and 8 and are unpatentable using the same analysis of claims

1-2 and 8.

8-8.   Claim 15 is a computer system claim including equivalent method limitations as in claim

1 and is unpatentable using the same analysis of claim 1.

9.   Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the

combined teachings of Lauterbach, "Accelerating Architectural Simulation by Parallel Execution

of Trace Samples", Tech. Report SMLI TR-93-22, Sun Microsystems Laboratories, Inc.,

December 1993, pages 1-14, and Applicants' assertions as applied to claim 1 above, and further

in view of Ball, U.S. Patent 5,615,357 issued March 25, 1997.

9-1.   Regarding claim 3, Lauterbach fails to expressly disclose said checkpoints divide said

program into code fragments of random lengths.

Ball discloses a method for verifying processor performance, wherein "the trace file is

randomly sampled to produce relatively small segments of contiguous trace instructions".

It would have been obvious to one of ordinary skill in the art at the time the invention

was made to modify the teachings of Lauterbach to incorporate the teachings of Ball to obtain

the invention as specified in claim 3 because by applying the randomly sampling technique, the

accurate processor performance can be statistically predicted without running a comprehensive

evaluation.

9-2. Claim 13 is a computer readable media claim include same method limitations as in claim

3 and is unpatentable using the same analysis of claim 3.

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined

teachings of Lauterbach, "Accelerating Architectural Simulation by Parallel Execution of Trace

Samples", Tech. Report SMLI TR-93-22, Sun Microsystems Laboratories, Inc., December 1993,

pages 1-14, and Applicants' assertions as applied to claim 1 above, and further in view of

Challier et al., U.S. Patent 6,199,031 issued March 6, 2001, and filed August 31, 1998.

10-1. Regarding claim 7, Lauterbach fails to expressly disclose each of said low level

simulators is a register transfer level (RTL) model of said processor, written as one of (a) a

VHDL model of said processor and (b) a Verilog model of said processor. However, Applicants

assert, as shown in FIG. 1A and described in pages 1-2 of the specification, "Figure 1A is a

block diagram of a prior art processor validation system 100 using only a low level simulator

110" and "One type of low level simulator is the register transfer level (RTL) model of the

processor" because "The RTL model is a one hundred percent accurate representation of a

processor and is the same model used to design the processor".

Challier et al. disclose an interface system for testing and verifying the design of an ASIC

at different levels of abstraction, wherein the ASIC includes a processor entity (Challier,

abstract). Challier et al. further disclose ASIC model 201 is a VHDL based design and model

201 runs on top of simulator 205 (Challier, column 5, lines 47-57). In other words, Challier et al.

disclose an interface system for testing and verifying the design of an ASIC at different levels of abstraction by implementing low level simulators.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined teachings of Lauterbach and Applicants' assertions to incorporate the teachings of Challier et al. to obtain the invention as specified in claim 7 because Challier et al. disclose in detail implementing low level simulators, as suggested by Applicants' assertions.

Conclusion

11.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Reference to Bose, U.S. Patent 6,059,835 issued May 9, 2000, and filed June 13, 1997, is cited as disclosing a processor performance evaluation system and method.

Reference to Maturana et al., "Incas: A Cycle Accurate Model of UltraSPARC™", Proceedings of 1995 IEEE International Conference on Computer Design: VLSI in Computers and Processors, October 1995, pages 130-135, is cited as disclosing a cycle accurate model to provide accurate performance estimates.

12.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Herng-der Day whose telephone number is (703) 305-5269. The examiner can normally be reached on 8:30 - 17:00.
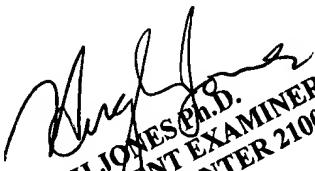
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 746-7239 for regular

communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day
September 30, 2003